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CANCEL CLAIMS 1-7

8. Arrangement with image sensors,

in which an image sensor has a memory transistor and a selection transistor, which are connected in series and between a bit line or a reference line,

in which a gate electrode of the selection transistor is connected to a word line, which extends crosswise in relation to the bit line,

in which the image sensor has a diode, which is switched between a gate electrode of the memory transistor and a first source/drain area of the memory transistor, which is connected to the selection transistor in such a way that it is polarised towards the first source/drain area of the memory transistor and in the reverse direction,

in which the image sensor has a photodiode, which is switched between a voltage connection and the gate electrode of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

9. Arrangement with image sensors,

in which an image sensor has a memory transistor and a selection transistor, which are connected in series and between a bit line and a reference line,

in which one gate electrode of the selection transistor is connected to a word line, which extends crosswise in relation to the bit line,

in which an image sensor has a diode, which is switched between a gate electrode of the memory transistor and a first source/drain area of the memory transistor, which is connected to the selection transistor in such a way that it is polarised towards the first source/drain area of the memory transistor and in the reverse direction,

in which an image sensor has a photodiode, which is switched between a voltage connection and the first source/drain area of the memory transistor in such a way that it is polarised towards the voltage connection and in the reverse direction.

10. Arrangement according to claim 8,

in which the photodiode consists of a n-doped area and a p-doped area adjacent to this, which is connected to the voltage connection.

11. Arrangement according to claim 10,

in which the n-doped area of the photodiode, the first source/drain area of the memory transistor and/or a first source/drain area of the selection transistor form a cohesive doped area.

12. Arrangement according to claim 8,

in which the memory transistor is designed as a vertical transistor,

in which the first source/drain area of the memory transistor is arranged over a second source/drain area of the memory transistor, which is connected to the reference line,

in which the reference line is buried in the substrate.

13. Arrangement according to claim 8,

in which the diode is designed as a tunnel diode and consists of the first source/drain area of the memory transistor, an insulating layer adjacent to this and a conductive structure adjacent to this, which is connected to the gate electrode of the memory transistor.

14. Arrangement according to claim 13,

in which one substrate has a recess,

in which the recess extends into the reference line,

in which at least one lateral face of an upper area of the recess is provided with the insulating layer,

in which faces of a lower area of the recess lying below the upper part are equipped with a gate insulator,

in which the gate electrode of the memory transistors is arranged in the lower part,

in which the conductive structure of the diode arranged is in the upper part of the recess,

in which the first source/drain area of the memory transistor is arranged in the substrate and is adjacent to the lateral face of the upper area.

15. Arrangement according to claim 9,

in which the photodiode consists of a n-doped area and a p-doped area adjacent to this, which is connected to the voltage connection.

16. Arrangement according to claim 15,

in which the n-doped area of the photodiode, the first source/drain area of the memory transistor and/or a first source/drain area of the selection transistor form a cohesive doped area.

17. Arrangement according to claim 9,

in which the memory transistor is designed as a vertical transistor,

in which the first source/drain area of the memory transistor is arranged over a second source/drain area of the memory transistor, which is connected to the reference line,

in which the reference line is buried in the substrate.

18. Arrangement according to claim 9,

in which the diode is designed as a tunnel diode and consists of the first source/drain area of the memory transistor, an insulating layer adjacent to this and a conductive structure adjacent to this, which is connected to the gate electrode of the memory transistor.

19. Arrangement according to claim 18,

in which one substrate has a recess,

in which the recess extends into the reference line,

in which at least one lateral face of an upper area of the recess is provided with the insulating layer,

in which faces of a lower area of the recess lying below the upper part are equipped with a gate insulator,

in which the gate electrode of the memory transistors is arranged in the lower part,

in which the conductive structure of the diode arranged is in the upper part of the recess,

in which the first source/drain area of the memory transistor is arranged in the substrate and is adjacent to the lateral face of the upper area.